DESCRIPTION

The Maestro1 PCI Audio Accelerator represents a new generation of architecture that not only meets the new demands of advanced PC audio applications but also enables the integration of a complete multimedia subsystem on either a single adapter or motherboard. Maestro1's functionality and interfaces are compliant with all major industry standards, including the Audio Subsystem Specification of PC97, Windows®95 DirectSound™, Windows® Sound System®, AC'97 CODEC Interface and PCI 2.1 Bus Specification.

The dual-engine architecture consisting of a 64-channel pipelined Wave Processor and a proprietary programmable Audio Signal Processor enables the Maestro1 to efficiently handle multiple audio streams of different types. This allows high-quality music synthesis, multiple PCM data streams at arbitrary sample rates, and voice compression and decompression to occur simultaneously.

The Maestro1 is available in an industry-standard 208-pin Plastic Quad Flat Pack (PQFP) package.

PCI Performance Audio

The PCI bus is required for PC audio hardware to smoothly reproduce high-fidelity sounds from internet, MIDI, WAV, and conferencing audio sources. It achieves high-performance functionality by reducing the actual transfer time of audio data and by enabling the transfer of multiple independent data streams. Compared to the ISA bus, PCI improves data transfer efficiency by at least 20 times. This is crucial for low-latency audio applications such as internet interactive audio. While providing a high-performance PCI interface, the Maestro1 retains full compatibility to existing DOS games through hardware emulation.

DirectSound Acceleration

The Maestro1 provides hardware acceleration of DirectSound data by digitally mixing up to 32 PCM streams and sample rate convert each individual stream from any frequency to 48 KHz. Hardware acceleration frees CPU mips to perform other tasks such as video processing.

Wavetable and Effect Synthesis

The Maestro1's 64-channel Wave Processor provides high-quality wavetable synthesis cost-effectively by storing the downloadable variable-sized table samples in system memory. With ESS Technology's WaveCache™ technology, the MIDI samples are fetched using the PCI bus during MIDI playback. Each channel has independently programmable pan, tremolo, vibrato and tone filtering. The WP is also capable of performing advanced audio effects such as reverb, chorus, flange, echo and 3-D spatial enhancement.

Legacy DOS Game Support

The Maestro1 achieves complete DOS game compatibility through three major schemes: PC/PCI DMA, Distributed DMA, and Transparent DMA. Transparent DMA requires no sideband signals and operates with all Pentium and Pentium Pro chipsets with no constraints.

FEATURES

- DOS Game compatibility
- 208-pin PQFP package

System Interface

- 32-bit PCI Bus Master, PCI 2.1 compliant
- < 0.5% PCI Bus Bandwidth for playing 16-bit/stereo/ 44.1KHz

Wavetable Synthesis

- 64-channel 50 MHz pipelined Wave Processor
- 1-8 MB Wavetable Memory downloadable in either system memory or local ROM/DRAM/SRAM/FlashROM
- Programmable pan, tremolo, vibrato, rate conversion and tone filtering per channel
- Programmable effects including reverb, chorus, flange, echo

DirectSound Acceleration

- Digital mixing up to 32 data streams
- Hardware sample rate convert to 48 KHz from any sample rate

3-D Sound

- 3-D positional audio under DirectX™ 5.0
- Enhanced effects (reverb, chorus, echo, vibrato, etc.)
- AC-3 decode acceleration
  - External DSP accelerates AC-3
  - Upgradeable to host-based algorithm

Software Compatibility

- Sound Blaster Pro
- Ad Lib
- Windows Sound System

- Windows 95
- DirectSound
- Microsoft® Active X

Hardware Interfaces

- MPU-401 interface with FIFO
- High-performance game port
- General-Purpose I/O port
- Communication interface port
- I²S digital audio Input
- Programmable audio CODEC interface:
  - PT-101 Audio CODEC
  - AC'97 CODEC Interface
  - Other 16-bit CODECs

CONTENTS

FIGURES

TABLES

MAESTRO1 ARCHITECTURE BLOCK DIAGRAMS

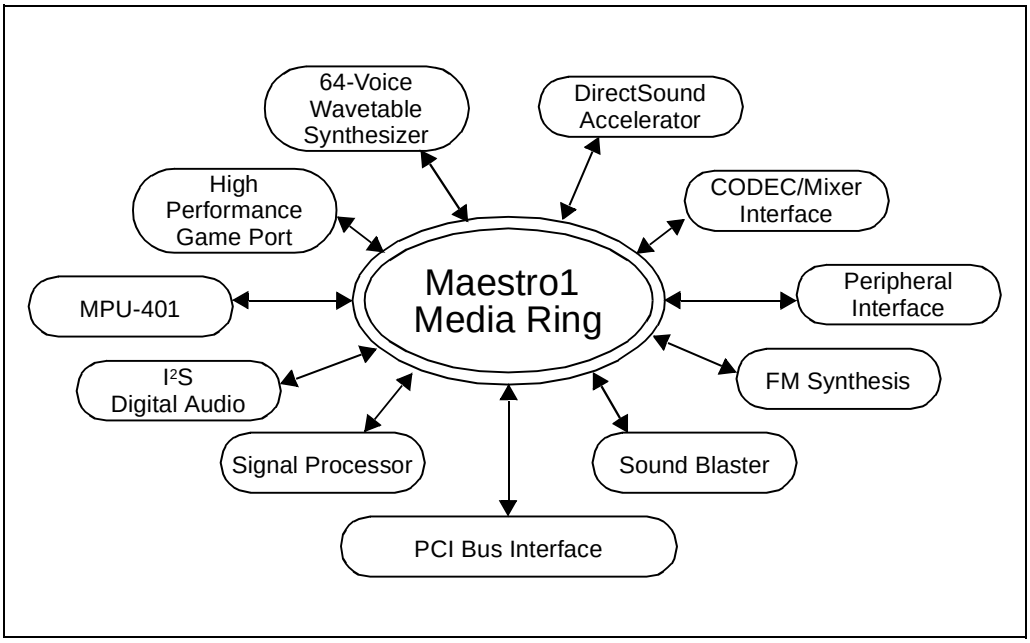


Figure 1 Maestro1 Block Diagram

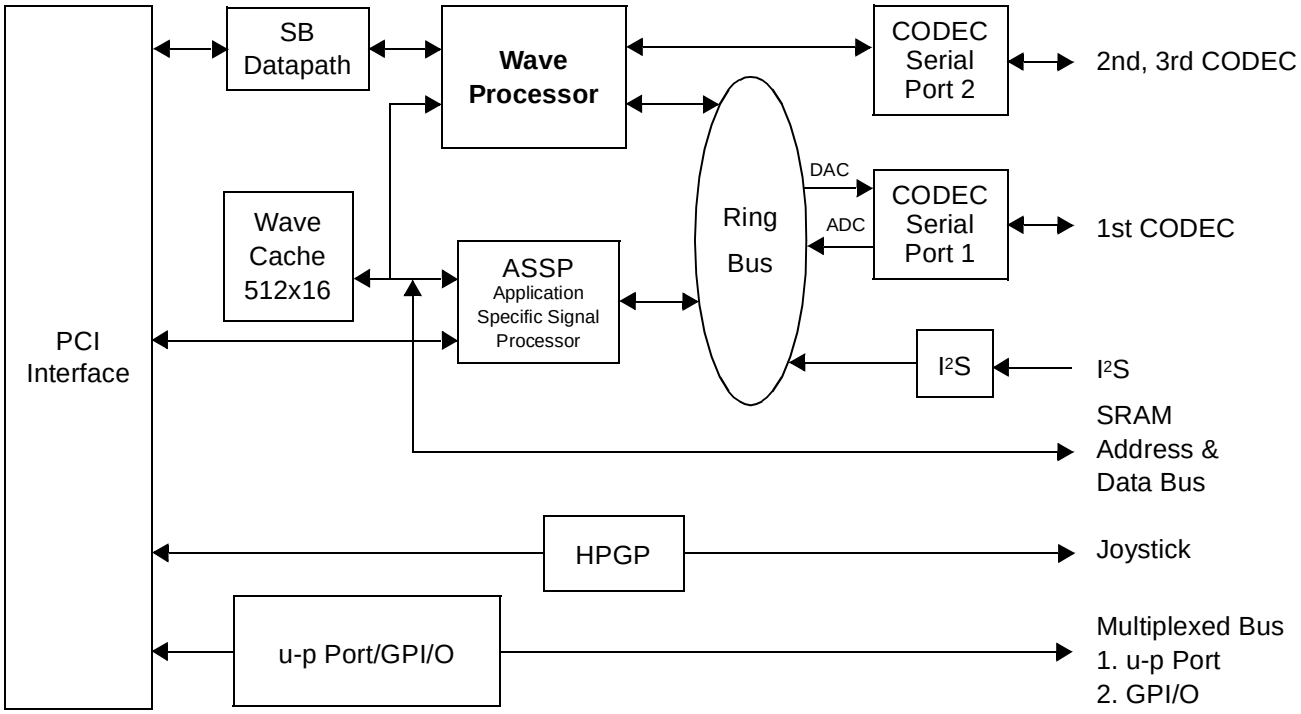


Figure 2 Maestro1 Architecture Block Diagram

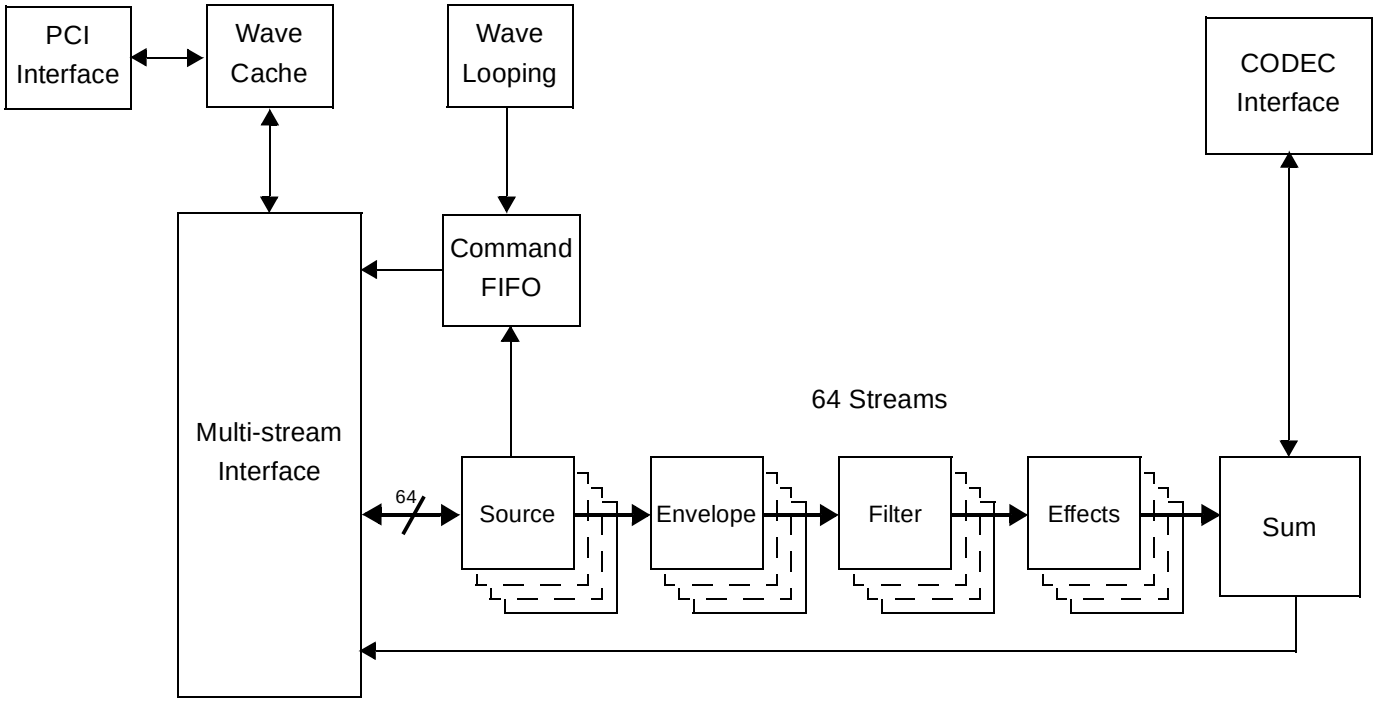


Figure 3 Wave Processor Portion

PINOUT

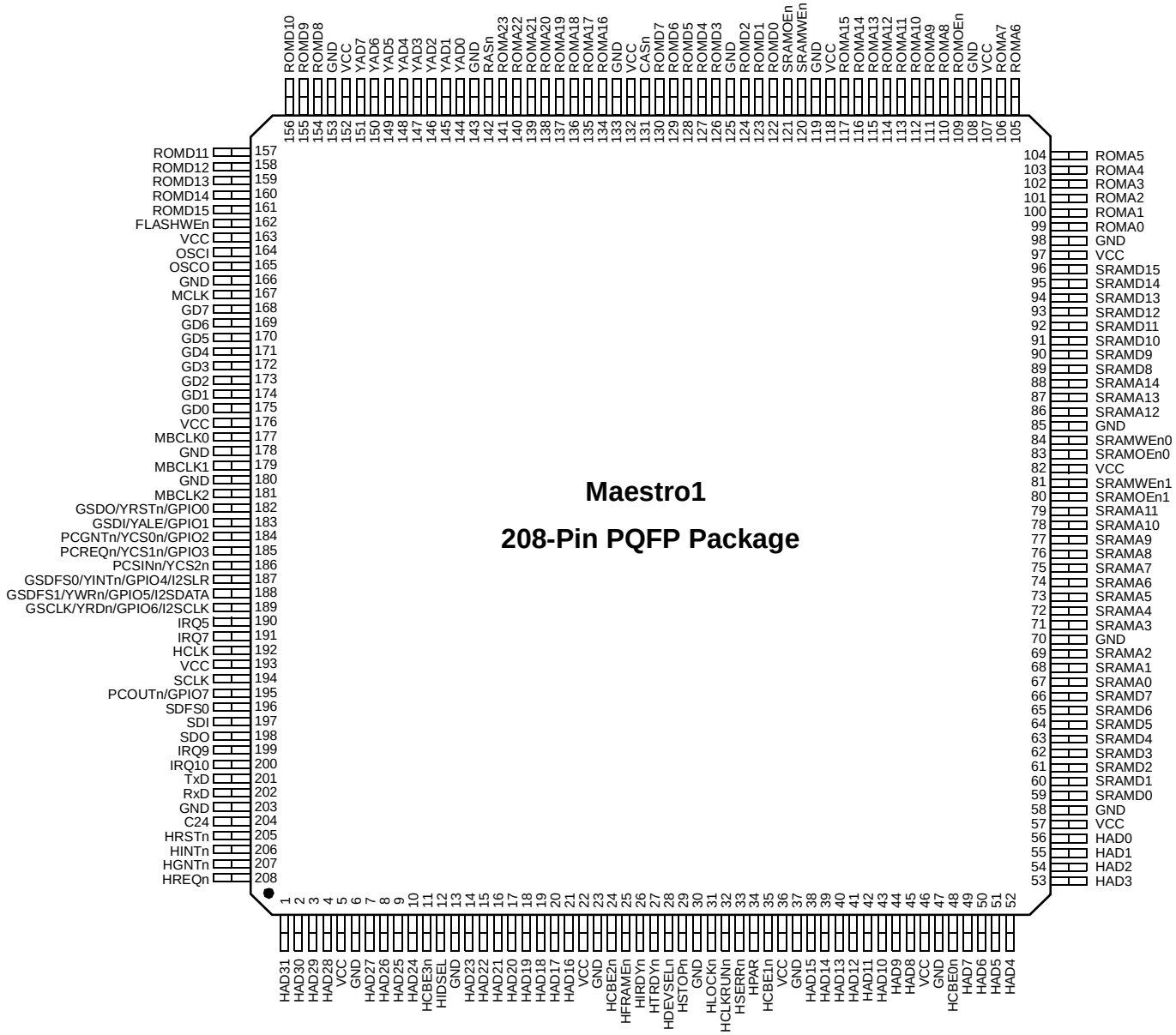


Figure 4 Maestro1 Pinout

PIN DESCRIPTION

O = Output - 24mA
Ob = Output - 4mA
Oc = Output - 24mA
PCI sustain output driver
Od = Output - 24mA. Open drain
Oe = Output - 8mA
Of = Output - 16mA
Og = Output - 24mA
I = Input - TTL
Ib = Input - CMOS Schmitt trigger
Ic = Input - TTL Schmitt trigger
Id = Input - CMOS Schmitt trigger with internal pull-up
Ie = Input - TTL with internal pull-up
If = Input - TTL Schmitt trigger with internal pull-up

Name	Number	I/O	Definition
Host Interface PCI Bus Pins (51)			
HAD[31:0]	1:4,7:10,14:21, 38:45,49:56	I/O	Multiplexed address and data lines
HCBE[3:0]n	11,24,35,48	I/O	Multiplexed command/byte enable
HRSTn	205	Ic	Reset
HPAR	34	I/O	Parity
HCLK	192	I	PCI bus clock
HFRAMEn	25	I/Oc	Cycle frame
HIRDYn	26	I/Oc	Initiator ready
HTRDYn	27	I/Oc	Target ready
HSTOPn	29	I/Oc	Stop transaction
HLOCKn	31	I/Oc	Lock
HIDSEL	12	I	ID select
HDEVSELn	28	I/Oc	Device select
HREQn	208	O	Request
HGNTn	207	I	Grant
HINTn	206	Od	Interrupt request
HSERRn	33	Od	System error
HCLKRUNn	32	I/Oc	Clock running
DRAM/SRAM/ROM Interfaces (58)			
YAD[7:0]	151:144	I/O	ISDN Access: YAD[7:0]
ROMA[23:0]	142:134,117:1 10,106:99	I/O	Either ROM or DRAM access. ROM = ROMA[23:0] DRAM = Reserved[23:12], DRAMA[11:0]
RASn	142	I/O	DRAM/SRAM control.
CASn	131	I/O	DRAM/SRAM control.
SRAMWEn	120	I/O	DRAM/SRAM control.
ROMOEn	109	I/O	ROM output enable.
ROMD[15:0]/ RAMD[15:0]	161:154,130:1 26,124:122	I/O	Either ROM (ROMD[15:0]: ROM data), or DRAM/SRAM (RAMD[15:0]: RAM data) access.
SRAMOEn	121	I/O	SRAM control.
FLASHWEn	162	O	Flash ROM control.
MCLK	167	I	MPCI bus clock
MBCLK[2:0]	181,179,177	O	Buffered MPCI bus clocks
AC'97 CODEC Interface (4)			

Name	Number	I/O	Definition
SCLK	194	I/Oe	Serial clock. Default is output. Pull SRAMA[1] low to set to the input. Must be less than 24.576 Mhz. Tentatively, this frequency is set at 12.5 Mhz (should be within the range of 10-15 Mhz). Data is transmitted after a rising edge of SCLK, and sampled on a falling edge of SCLK.
SDFS0	196	Oe	Serial data frame sync. New data frames are marked by a LO to HIGH transition on SDFS0 one serial clock period before the frame begins. The transition back from HI to LO may occur at any time provided the HI and LO times of SDFS0 are at least one SCLK period in duration each.
SDI	197	I	Serial data in
SDO	198	Oe	Serial data out
IRQ Pins (4)			
IRQ5	190	Og	ISA IRQ5
IRQ7	191	Og	ISA IRQ7
IRQ9	199	Og	ISA IRQ9
IRQ10	200	Og	ISA IRQ10
MPU-401 Interface (2)			
TxD	201	O	MIDI transmit data
RxD	202	Ic	MIDI receive data
Game Port Interface (8)			
GD[7:4]	168:171	Id	Game port data
GD[3:0]	172:175	Ib/O	Game port data
Clocks (3)			
OSCI	164	I	49.152 MHz crystal input
OSCO	165	Ob	49.152 MHz crystal output
C24	204	Ob	24.576 MHz clock output. For CODEC clock source.
SRAM Interface (35)			
SRAMA[14:11]	88:86,79	Ie/Oe	SRAM address. SRAMA[14:11] is at input state only during the Reset period. Inputs are latched during reset to define Bit [15:13] and Bit [8] of 16-bit Subsystem ID at the offset 2Eh of PCI Config. Space.
SRAMA[10]	78	Ie/Oe	SRAM address. SRAMA10 is at input state only during the Reset period. If NC (with internal pull-up): second CODEC is disabled. If 0: Enable second CODEC.
SRAMA[9:2]	77:71,69	Ie/Oe	SRAM address. SRAMA[9:2] is at input state only during the Reset period. Inputs are latched during reset to define Bit [7:0] of 16-bit Subsystem ID at the offset 2Eh of PCI Config. Space.
SRAMA[1]	68	Ie/Oe	SRAM address. SRAMA1 is at input state only during the Reset period. If NC (with internal pull-up): SCLK = Output. If 0: SCLK = Input.
SRAMA[0]	67	Ie/Oe	SRAM address. SRAMA0 is at input state only during the Reset period. Pull this pin low to enable local DRAM interface.
SRAMD[15:0]	96:89,66:59	I/Ob	SRAM data.

Name	Number	I/O	Definition
SRAMOEn[1:0]	80,83	Ie/Ob	SRAM output enable. SRAMOEn[1:0] is at input state only during the Reset period. Inputs are latched during reset to define Bit [9] and Bit [11] of 16-bit Subsystem ID at the offset 2Eh of PCI Config. Space.
SRAMWEn[1:0]	81,84	Ie/Ob	SRAM write enable. SRAMWEn[1:0] is at input state only during the Reset period. Inputs are latched during reset to define Bit [10] and Bit [12] of 16-bit Subsystem ID at the offset 2Eh of PCI Config. Space.
Second CODEC Interface (5)			
GSCLK *	189	Oe	Multipurpose pin. GSCLK, YRDn, GPIO6, or I2SCLK. When used as GSCLK = serial clock. Must be less than 24.576 Mhz. Data is transmitted after a rising edge of SCLK.
GSDFS0 *	187	Oe	Multipurpose pin. GSDFS0, YINTn, GPIO4, or I2SLR. When used as GSDFS0 = serial data frame sync 0. New data frames are marked by a LO to HIGH transition on SDFS0 one serial clock period before the frame begins. The transition back from HI to LO may occur at any time provided the HI and LO times of SDFS0 are at least one SCLK period in duration each.
GSDFS1 *	188	Oe	Multipurpose pin. GSDFS1, YWRn, GPIO5, or I2SDATA. When used as GSDFS1 = serial data frame sync 1. New data frames are marked by a LO to HIGH transition on SDFS1 one serial clock period before the frame begins. The transition back from HI to LO may occur at any time provided the HI and LO times of SDFS1 are at least one SCLK period in duration each.
GSDI *	183	Ie	Multipurpose pin. GSDI, YALE, or GPIO1. When used as GSDI = serial data in.
GSDO *	182	Q	Multipurpose pin. GSDO, YRSTn, or GPIO0. When used as GSDO = serial data out.
PC/PCI Interface (4)			
PCGNTn *	184	Ie	Multipurpose pin. PCGNTn, YCS0n, or GPIO2. When used as PCGNTn = PC/PCI grant.
PCREQn *	185	Oe	Multipurpose pin. PCREQn, YCS1n, or GPIO3. When used as PCREQn = PC/PCI request.
PCSINn *	186	Ie/Ob	Multipurpose pin. PCSINn, or YCS2n. When used as PCSINn = PC/PCI serial IRQ input. COMPAQ: serial IRQ input/output
PCOUTn *	195	Oe	Multipurpose pin. PCOUTn, or GPIO7. When used as PCOUTn = PC/PCI serial IRQ output.
Peripheral/ISDN Interface (8)			
YRSTn *	182	Oe	Multipurpose pin. GSDO, YRSTn, or GPIO0. When used as YRSTn = reset. A “low” on this pin forces both LAPD and LAPB devices into reset state. The minimum pulse length is 1.8 µs.
YALE *	183	Oe	Multipurpose pin. GSDI, YALE, or GPIO1. When used as YALE = address latch enable. A “high” on this pin indicates an address valid on the multiplexed address/data bus (AD7-0).
YCS0n *	184	Oe	Multipurpose pin. PCGNTn, YCS0n, or GPIO2. When used as YCS0n = chip select 0. A “low” on this line selects LAPD device for read/write operation.
YCS1n *	185	Oe	Multipurpose pin. PCREQn, YCS1n, or GPIO3. When used as YCS1n = chip select 1. A “low” on this line selects LAPB device for read/write operation.
YCS2n *	186	Oe	Multipurpose pin. PCSINn, or YCS2n. When used as YCS2n = chip select 2. A “low” on this line selects U interface device for read/write operation.
YINTn *	187	Ie	Multipurpose pin. GSDFS0, YINTn, GPIO4, or I2SLR. When used as YINTn = interrupt. This pin is shared by both LAPD and LAPB devices.
YWRn *	188	Oe	Multipurpose pin. GSDFS1, YWRn, GPIO5, or I2SDATA. When used as YWRn = write. Active-low. This signal indicates a write operation. It is common to both LAPD and LAPB devices
YRDn *	189	Oe	Multipurpose pin. GSCLK, YRDn, GPIO6, or I2SCLK. When used as YRDn = read. Active-low. This signal indicates a read operation. It is common to both LAPD and LAPB devices.
General-Purpose I/O Pins (7)			

Name	Number	I/O	Definition
GPIO0 *	182	Ie/Oe	Multipurpose pin. GSDO, YRSTn, or GPIO0. When used as GPIO0 = GPIO0.
GPIO1 *	183	Ie/Oe	Multipurpose pin. GSDI, YALE, or GPIO1. When used as GPIO1 = GPIO1.
GPIO2 *	184	Ie/Oe	Multipurpose pin. PCGNTn, YCS0n, or GPIO2. When used as GPIO2 = GPIO2.
GPIO3 *	185	Ie/Oe	Multipurpose pin. PCREQn, YCS1n, or GPIO3. When used as GPIO3 = GPIO3.
GPIO4 *	187	Ie/Oe	Multipurpose pin. GSDFS0, YINTn, GPIO4, or I2SLR. When used as GPIO4 = GPIO4.
GPIO5 *	188	Ie/Oe	Multipurpose pin. GSDFS1, YWRn, GPIO5, or I2SDATA. When used as GPIO5 = GPIO5.
GPIO6 *	189	Ie/Oe	Multipurpose pin. GSCLK, YRDn, GPIO6, or I2SCLK. When used as GPIO6 = GPIO6.
GPIO7 *	195	Ie/Oe	Multipurpose pin. PCOUTn, or GPIO7. When used as GPIO7 = GPIO7.
I²S Interface (3)			
I2SLR *	187	Ie	Multipurpose pin. GSDFS0, YINTn, GPIO4, or I2SLR. When used as I2SLR = I²S left right latch.
I2SDATA *	188	Ie	Multipurpose pin. GSDFS1, YWRn, GPIO5, or I2SDATA. When used as I2SDATA = I²S data input pin.
I2SCLK *	189	Ie	Multipurpose pin. GSCLK, YRDn, GPIO6, or I2SCLK. When used as I2SCLK = I²S clock.
Power Pins (34)			
VCC	5,22,36,46,57, 82,97,107,118, 132,152,163, 176,193	Pwr	+5 volts
GND	6,13,23,30,37, 47,58,70,85, 98,108,119, 125,133,143, 153,166,178, 180,203	Pwr	Ground

* These pins share more than one function.

PCI CONFIGURATION REGISTERS

Register Summary

Table 1 PCI Configuration Registers Summary

Reg					Remark
00h	Device ID (reserved)		Vendor ID (reserved)		
04h	Status		Command		
08h	Base class code (reserved)	Sub-class code (reserved)	Programming interface identifier (reserved)	Revision ID (reserved)	
0Ch	Reserved	Header type (reserved)	Latency timer	Reserved	
10h	Reserved				
14h	Reserved				
18h	Reserved				
1Ch	Reserved				
20h	Reserved				
24h	Reserved				
28h	Reserved				
2Ch	Subsystem ID (reserved)		Subsystem vendor ID (reserved)		
30h	Reserved				
34h	Reserved				
38h	Reserved				
3Ch	Max_Lat (reserved)	Min_Gnt (reserved)	Interrupt pin (reserved)	Interrupt line	

All reserved locations are Read-only with a default value of zero.

Register Descriptions

Vendor ID (00h, 01h, R)

Vendor ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Vendor ID	Identifies ESS as the manufacturer of this device. The ID for ESS is 1285h.

Device ID (02h, 03h, R)

Device ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Device ID	Identifies Maestro1 as this device. This ID 0100h is assigned by ESS Technology, Inc.

Command (04h, 05h, R/W)

0	0	0	0	0	0	0	0	0	0	0	0	0	BM	MS	IO
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:3	–	Reserved. Always write 0.
2	BM	Bus Master enable/disable. 1 = Enable bus master. 0 = Not bus master.
1	MS	Memory Space access enable/disable. 1 = Enable memory space access. 0 = Disable memory space access.
0	IO	I/O Space access enable/disable. 1 = Enable I/O space access. 0 = Disable I/O space access.

Status (06h, 07h, R/W)

0	0	MA	TA	0	TS		0	FB	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:14	–	Reserved. Always write 0.
13	MA	Received master abort. To clear, write a 1 to this bit.
12	TA	Received target abort. To clear, write a 1 to this bit.
11	–	Reserved. Always write 0.
10:9	TS	DEVSELn timing status. This device is set to 01 for medium timing. This location is read-only.
8	–	Reserved. Always write 0.
7	FB	Fast Back-to-back capable. Hard wired 1.
6:0	–	Reserved. Always write 0.

Revision ID (08h, R)

Revision ID							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	Revision ID	Identifies the revision of this device. This ID 10h is assigned by ESS Technology, Inc.

Programming Interface Identifier (09h, R)

Programming interface identifier							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	PII	Identifies the programming interface of this device. This ID 00h is assigned by ESS Technology, Inc. as a default interface.

Sub-Class Code (0Ah, R)

Sub-class code							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	SCC	Identifies the type of sub-class of this device. This ID 01h is assigned by ESS Technology, Inc. as an audio device.

Base Class Code (0Bh, R)

Base class code
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	BCC	Identifies the type of base class of this device. This ID 04h is assigned by ESS Technology, Inc. as a multimedia device.

Latency Timer (0Dh, R/W)

LT				0	0	0	0
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	LT	Number of clocks times 16.
3:0	–	Reserved. Always write 0.

Header Type (0Eh, R)

SM	Configuration space layout						
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	SM	Single/Multifunction device. The value is set by the SRAMA0 pin, when sampled during reset: N.C. (with internal pull-up) = this device is a multifunction device. The MPCI pins are set to Multimedia PCI mode. 0 = This device is a single-function device. The MPCI pins are set to Wavetable Memory Mode (ROM/DRAM).
6:0	CSL	Configuration space layout. Defines layout for bytes 10h and up of the PCI configuration space header. Maestro1 supports a 00h header type.

Subsystem Vendor ID (2Ch, 2Dh, R)

Subsystem vendor ID
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:0	Subsystem vendor ID	Identifies the subsystem vendor ID of this device. This ID 1285h is assigned by ESS Technology, Inc.

Subsystem ID (2Eh, 2Fh, R)

Subsystem ID
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:0	Subsystem ID	Identifies the subsystem ID of this device. This ID is generated from strap input pins of SRAMA[14:12], SRAMWEn[1:0], SRAMOEn[1:0], SRAMA11, and SRAMA[9:2].

Interrupt Line (3Ch, R/W)

Interrupt Line
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	Interrupt line	Interrupt line routing information. Indicates which system interrupt pin the Maestro1 is connected to. The POST software writes the routing information to the Interrupt Line register as the system is initialized and configured. The value in this register depends on the system architecture. In x86-based PC system, the values of 0 to 15 correspond with the IRQ numbers 0 through 15, and the values from 16 to 254 are reserved. The value of 255 (the Maestro1's default power-up value) signifies either "unknown" or "no connection" for the system interrupt.

Interrupt Pin (3Dh, R)

Interrupt pin
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	Interrupt pin	Interrupt pin information. Indicates which interrupt pin the Maestro1 is using. The value is 01h, which corresponds to INTAn.

Minimum Grant (3Eh, R)

Minimum grant
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	Minimum grant	Min_Gnt. Identifies the burst period needed. The value is 02h, which corresponds to 500 ns.

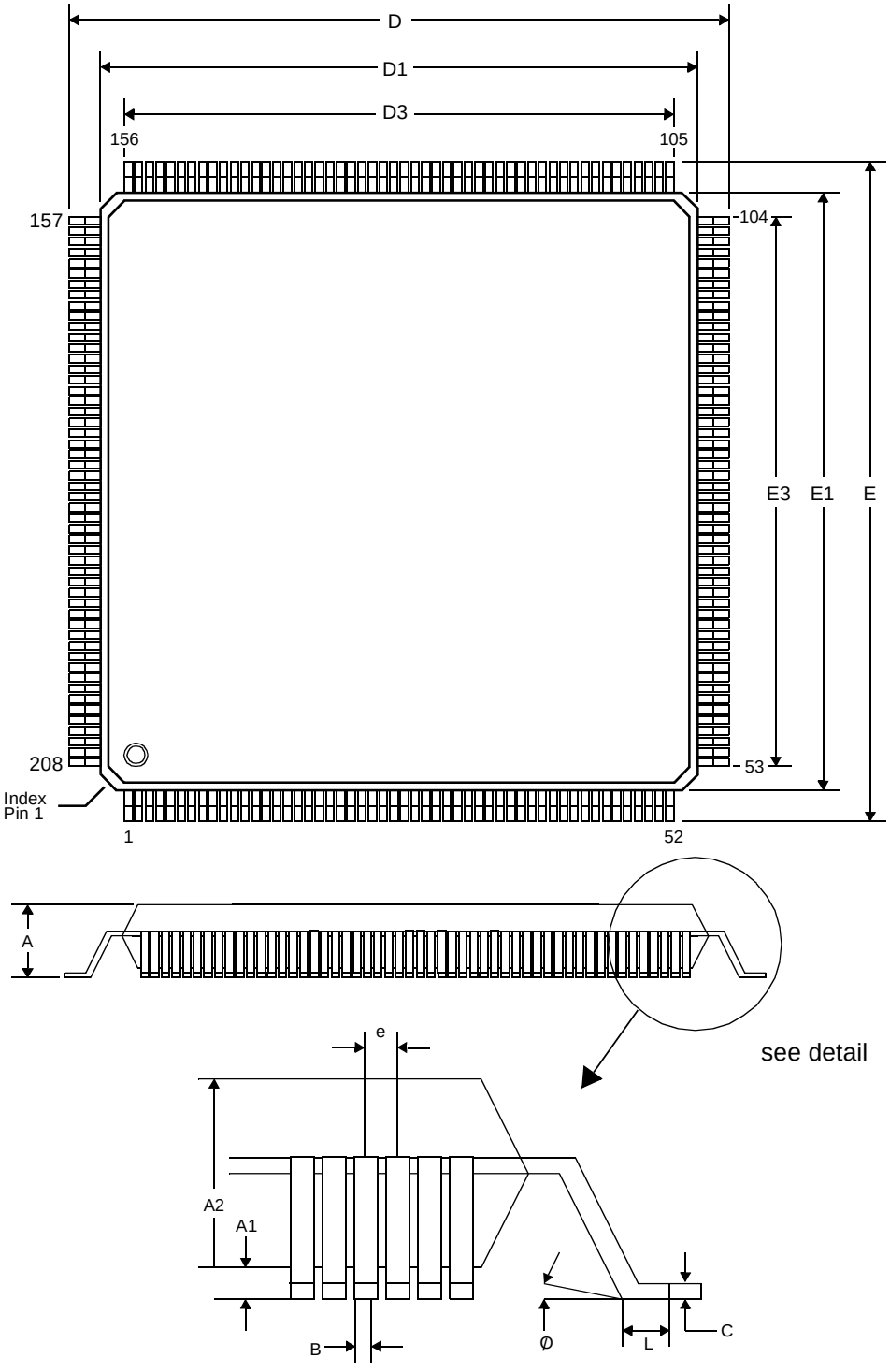
Maximum Latency (3Fh, R)

Maximum latency							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	Maximum latency	Max_Lat. Identifies how often bus access is needed. The value is 18h, which corresponds to 6 ms.

MECHANICAL DIMENSIONS



Note:
1. All dimensions are in inches (millimeter).
2. Actual package used has millimeter native dimensions – take care with rounding from metric to imperial.

Symbol	Min	Nom	Max
A	–	–	0.165
A1	0.010 (0.25)	–	–
A2	0.130 (3.30)	0.134 (3.40)	0.138(3.50)
B	0.007 (0.18)	0.009 (0.23)	0.011 (0.28)
C	0.005 (0.12)	0.006 (0.16)	0.008 (0.20)
D	1.195 (30.35)	1.205 (30.60)	1.215 (30.85)
D1	1.098 (27.90)	1.102 (28.00)	1.106 (28.10)
D3	1.004 (25.50) REF		
e	0.0197 (0.50) BASIC		
E	1.195 (30.35)	1.205 (30.60)	1.215 (30.85)
E1	1.098 (27.90)	1.102 (28.00)	1.106 (28.10)
E3	1.004 (25.50) REF		
L	0.016 (0.40)	0.020 (0.50)	0.024 (0.60)
φ	0i	2.5i	5.0I

Figure 5 Maestro1 Mechanical Dimensions

ELECTRICAL CHARACTERISTICS

Table 2 Digital Characteristics

Parameter	Symbol	Min	Max	Unit
Input voltage high: all digital inputs except Xtal[2:1]	VIH	2.4	Vdd+0.3	V
Input Voltage high: Xtal[2:1]	VIH2	2.4	Vdd+0.3	V
Input voltage low: all digital inputs	VIL	-0.3	0.8	V
Output voltage high	VOH	2.4		V
Output voltage low	VOL		0.4	V
Input leakage current		-10	10	µA
Output leakage current		-10	10	µA

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Revision History

REV	Changes
A	Initial preliminary document.

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Document Number: SAM0050A
May 1997